

# Sidewall depletion in nano-patterned LAO/STO heterostructures

M. Z. Minhas,<sup>1</sup> H. H. Blaschek,<sup>1</sup> F. Heyroth,<sup>2</sup> and G. Schmidt<sup>1,2,\*</sup>

<sup>1</sup>*Institut für Physik, Martin-Luther-Universität Halle-Wittenberg, Von-Danckelmann-Platz 3, D-06120 Halle, Germany*

<sup>2</sup>*Interdisziplinäres Zentrum für Materialwissenschaften,  
Martin-Luther-Universität Halle-Wittenberg, Heinrich-Damerow-Str. 4, 06120 Halle, Germany*

We report the fabrication of nanostructures from the quasi-two-dimensional electron gas (q2DEG) formed at the  $\text{LaAlO}_3/\text{SrTiO}_3$  (LAO/STO) interface. The process uses electron beam lithography in combination with reactive ion etching. This technique allows to pattern high-quality structures down to lateral dimensions as small as 100nm while maintaining the conducting properties without inducing conductivity in the STO substrate. Temperature dependent transport properties of patterned Hall bars of various widths show only a small size dependence of conductivity at low temperature as well as at room temperature. The deviation can be explained by a narrow lateral depletion region. All steps of the patterning process are fully industry compatible.

The discovery of an electron gas at the interface between the two band insulators  $\text{LaAlO}_3$  (LAO) and  $\text{SrTiO}_3$  (STO)[1, 2] has initiated a huge effort to study this interface in detail. Besides the interface conductivity also other interesting properties have been reported such as induced ferromagnetism at the interface between the two non-magnetic insulating perovskites[3] and superconductivity below 200 mK. [4, 5] To understand the origin of the electrical conductivity different models have been proposed; polar discontinuity at the interface,[6] formation of oxygen vacancies in the STO substrate during the growth of LAO on STO substrate,[7–9] or La-Sr intermixing at the interface. [10] Due to the above mentioned properties the LAO/STO interface has not only become a model system to study the fundamental physics of strongly correlated electronic systems but also a candidate for future multifunctional oxide electronics. [11, 12]

Still one challenge has to be faced. For both, using the material in nanopatterned quantum transport devices or employing it in state of the art field effect transistor based nanoelectronics a reliable and reproducible patterning technique is essential to achieve lateral insulation between devices. Common dry etching techniques like Ar ion milling are of only limited use for LAO/STO structures, because exposure to the ion beam creates a highly conducting layer on the  $\text{SrTiO}_3$  substrate surface at room temperature as well as at cryogenic temperatures.[13–15] This highly conducting layer complicates any transport experiment in the patterned structures and makes device applications virtually impossible. Up to now, however, a number of indirect patterning processes have been reported. One successful approach for patterning makes use of the particular thickness dependence of the interface conductivity, which sets in when the thickness of the LAO layer exceeds 4 unit cells (u.c.) only. In this approach of Schneider et al.[16] 2u.c of epitaxial LAO were grown on STO substrate. Subsequently UV-lithography was done and amorphous LAO was deposited which was then patterned by lift off. Further deposition of LAO under suitable growth conditions led to a continuation of epitaxial growth limited to those places where the epitaxial LAO surface was still open while in places covered by amorphous material crystalline growth was inhibited. In places where epitaxial growth occurred the condition for a conducting interface was fulfilled. Thus a patterning of the conductivity without physical patterning of the interface was achieved. In another approach Banerjee et al.[17] used an  $\text{AlO}_x$  based hard mask and epitaxial lift-off, leaving the desired areas of LAO/STO with insulating STO in between. In their approach, however, no nanopatterning was demonstrated and the STO substrate was exposed to lithography and solvents before the deposition of LAO. While these two processes used epitaxial growth on the pre-patterned surfaces there were also attempts to locally modify the conductivity in large area LAO/STO layers.

Quite frequently conducting atomic force microscope (AFM) probes were used to create and erase conducting nanoscale structures at the LAO/STO interface. Quantum size effect could be demonstrated, [18, 19] however, the disadvantage of this technique is that the structures are not stable over time at ambient conditions and it is difficult to pattern large area devices or even integrated circuits by using this technique. Recently, low energy Ar-ion beam irradiation was used to pattern the quasi-two-dimensional electron gas (q2DEG) at the LAO/STO interface with the combination of optical and electron beam lithography and subsequent ion beam irradiation. [20] The process relies on the fact that the decrease in interface conductivity under ion radiation due to lattice damage is faster than the increase of the substrate conductivity, leaving only a small process window for pattern fabrication. Lateral dimensions of 50nm were achieved, however, at the cost of an unexplained increase in resistivity of almost one order of magnitude. No real physical nano-patterning of large area LAO/STO has been reported so far because of the issue of ion induced conductivity of the STO surface.

Here we present a reliable technique to physically pattern the q2DEG down to lateral dimensions as small as 100nm while maintaining its conducting properties, however, without the problem of an ion induced substrate conductivity.

We use LAO layers (6.u.c) grown by pulsed laser deposition (PLD) from a single crystal LAO target on  $\text{TiO}_2$ -terminated STO (001) substrates.[21–23] Oxygen is used as a background gas at a pressure of  $10^{-3}$  mbar during the deposition. The substrate temperature during deposition is 850°C. Laser fluence and pulse frequency are kept at 2 J/cm<sup>2</sup> and 2Hz, respectively, during the deposition. To monitor the layer thickness up to unit cell level in situ reflection high-energy electron diffraction (RHEED) is used during the growth.[24] After deposition the samples are slowly cooled down to room temperature while the oxygen pressure is maintained.

For the patterning a thin film of novolack based image reversal resist is deposited by spin coating (see Fig. 1, left). Subsequently the sample is exposed by electron beam (e-beam) lithography. The resist we use is also suitable for high resolution optical lithography allowing for direct transfer of the process to industrial lithography tools. The exposed pattern consists of Hall bars with different respective nominal width between 100 and 500nm including large area bond pads. After development reactive ion etching is performed in an Inductively coupled plasma reactive ion etching system (ICP-RIE, Oxford Plasmalab 100). The etching process uses a pressure of 5 mTorr of  $\text{BCl}_3$ . The plasma is excited with a combination of RIE and ICP at a total power of 1430W. The sample temperature is kept at 5°C by helium backside cooling. Using these parameters we achieve an etch rate of  $13 \pm 3 \text{ nm/min}$ . We chose a process time of 19 s in order to completely remove the LAO layer. After the etching the resist is removed using N-Ethylpyrrolidone at 60°C for 3 hours. The resulting patterned structures are stable at ambient conditions. The Hall bars are bonded using Al wire for electrical transport measurements. The bonds are placed directly on the LAO without additional metallization. Fig. 1 (right) shows a 100 nm wide bar with approx. 500 nm wide contact leads.

Electrical transport measurements are carried out in a <sup>4</sup>He bath cryostat in the temperature range of 4.2 – 300K. We are using DC measurements with a voltage drop over the sample of approximately 5 – 7mV. The voltage drop over the sample and the reference resistor, respectively, as well as the Hall voltage are measured using high impedance difference amplifiers and an Agilent 34420A nanovoltmeter. All fabricated Hall bars show metallic behavior down to 4.2K (see Fig. 2). The area between

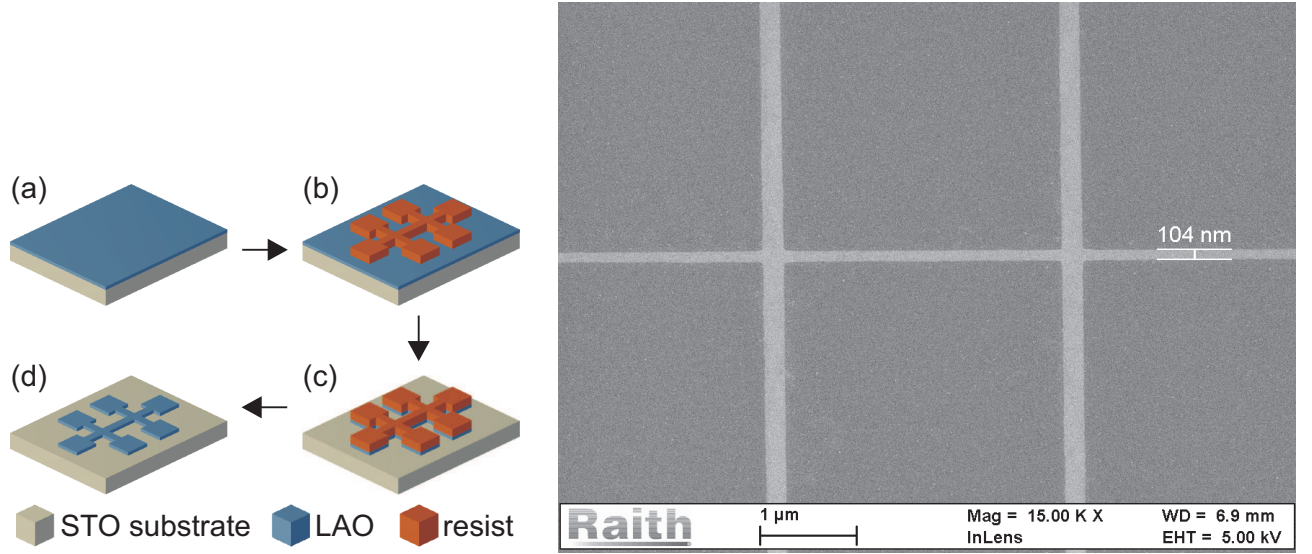


FIG. 1: Left: Schematic diagram showing the process used to pattern the q2DEG down to nanometer scale. (a) The LAO film is deposited on the  $TiO_2$ -terminated STO substrate. (b) Resist is deposited and patterned by e-beam lithography. (c) Dry etching is performed down to the STO substrate. (d) After removal of the resist, the patterned LAO structure remains on the STO. Right: Scanning electron micrograph of part of a 100 nm wide Hall bar with approx. 500 nm wide contact leads at the top and bottom.

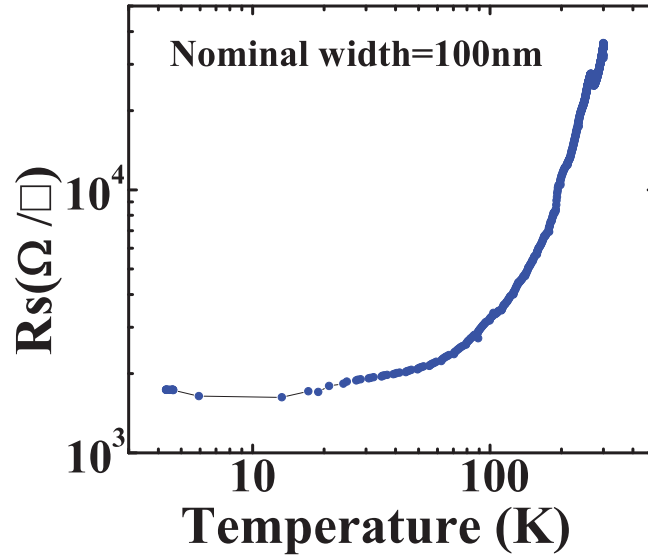


FIG. 2: Temperature dependent sheet resistance of the q2DEG in Hall bar geometry with a nominal width of 100nm.

the structures is insulating at room as well as at low temperature. Fig. 3(a and b) shows the resistance as a function of the Hall bars inverse nominal width at room as well as at low temperature. Although the plots show almost straight lines as expected for constant conductivity, there is a notable increase in sheet resistance with decreasing dimension of the structures. This effect can be seen more precisely when the sheet resistance is plotted as a function of width (see Fig. 4). For a perfect etching process the sheet resistance should be constant and independent from the width of the Hall bars. In our results, however, comparing the temperature dependent resistivity for large area sample and micro Hall bars of different widths yields the following: For large area samples the sheet resistance is approximately  $12\text{K}\Omega/\square$  at room temperature and  $0.2\text{K}\Omega/\square$  at 4.2K. In the Hall bars we observe a slight increase in sheet resistance with decreasing width. This increase, however, is much weaker than the one observed by Aurino et al.[20]. In order to understand the origin of the effect we analyze the dependence of the resistance on the width of the structures in more detail. While an overall increase of the resistivity of the nanopatterned samples does not fit the

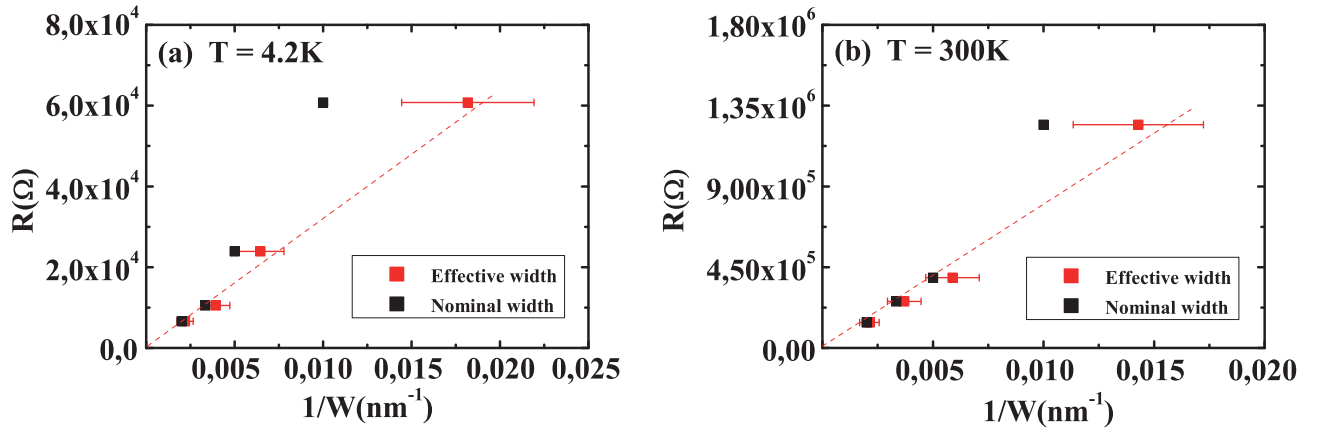


FIG. 3: Resistance of the q2DEG in Hall bar geometry plotted as a function of the inverse effective (red) and nominal (black) width of the Hall bars. (a) Measured at 4K, (b) measured at 300K.

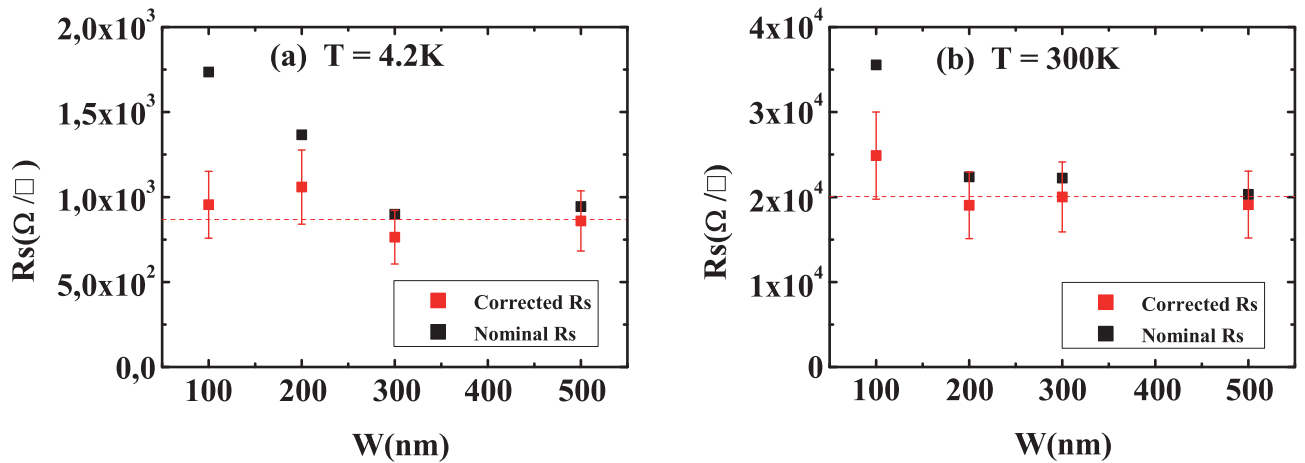


FIG. 4: Sheet resistance of the q2DEG in Hall bar geometry plotted as a function of width. When the effective width is used, the sheet resistance is constant within the error bars. (a) Measured at 4K, (b) measured at 300K.

experimental results, side wall damage can explain the observations.

During the etching process, the sidewalls are exposed to the etchant and the material is damaged to a certain extent, mainly depending on the etching time. As the etching time is constant for all structures, the depth of the damage in the crystal is also identical for all Hall bars. This damage can result in a non-conducting depletion region with constant width for all structures. If this assumption is true introducing an 'effective' width for the Hall bars in which a constant value 'x' is subtracted from the nominal width should yield a constant sheet resistance for all Hall bars. For the sake of simplicity we assume an infinite resistance for the depletion region. The sidewall depletion length x can be found by fitting Hall bars of different width to the formula:

$$R_{total} = \frac{\rho_1 \rho_2 L}{\rho_2 t_1 w - x(\rho_2 t_1 - \rho_1 t_2)} \quad (1)$$

where  $\rho_1$  and  $\rho_2$  are electrical resistivity and 'w' and 'x' is width of Hall bar and depletion region respectively. It should be noted that the width of the depletion region is expected to depend on the temperature and thus for the fitting procedure two different respective depletion regions must be assumed for  $T=4.2\text{ K}$  and for the room temperature. This assumption takes into account that defects introduced by the etching may be traps whose occupation depends on the energy level and thus on the temperature. Based on this analysis we get a best fit for a side wall depletion of approximately  $15\text{ nm}$  on each side of structure at room temperature and  $20\text{ nm}$  at  $4.2\text{ K}$ . Fig. 4 shows the sheet resistance plotted over the nominal width once calculated using the nominal width and once calculated using the effective width. Obviously the value which is obtained using the effective width

is constant within the error bars of approximately 20% at 4.2 K as well as at room temperature confirming the validity of our model.

In conclusion we have demonstrated that it is possible to pattern the electron gas at the LAO/STO interface using e-beam lithography in combination with dry etching. The process preserves the conductivity of the electron gas but leaves the substrate insulating and thus can be used for the lateral insulation of electrical devices. Our analysis shows that a small depletion region is induced at the lateral surfaces which reduces the effective width of the structures. Nevertheless, the resolution is good enough to access device dimensions well below 100 nm. Using a Novolac based resist which is also suitable for optical lithography and ICP and RIE based reactive chemical dry etching the process is industry compatible and it is expected that more detailed optimization of the process conditions can even further reduce the already small surface damage.

## ACKNOWLEDGMENTS

This work was supported by the European Commission in the project IFOX under grant agreement NMP3-LA-2010-246102 and by the DFG in the SFB 762.

---

\* Correspondence to G. Schmidt: georg.schmidt@physik.uni-halle.de

- [1] A. Ohtomo and H. Y. Hwang, *Nature*. **427**, 423 (2004)
- [2] S. Thiel, G. Hammerl, A. Schmehl, C. W. Schneider, and J. Mannhart, *Science*. **313**, 1942 (2006)
- [3] A. Brinkman, M. Huijben, M. V. Zalk, J. Huijben, U. Zeitler, J. C. Maan, W. G. Van der Wiel, G. Rijnders, D. H. A. Blank, and H. Hilgenkamp, *Nature Materials*. **6**, 493 (2007)
- [4] N. Reyren, S. Thiel, A. D. Caviglia, L. F. Kourkoutis, G. Hammerl, C. Richter, C. W. Schneider, T. Kopp, A. S. Rüetschi, D. Jaccard, M. Gabay, D. A. Muller, J. M. Triscone, and J. Mannhart, *Science*. **317**, 1196 (2007)
- [5] L. Li, C. Richter, J. Mannhart, and R. C. Ashoori, *Nature Physics*. **7**, 762 (2011)
- [6] N. Nakagawa, H. Y. Hwang, and D. A. Muller, *Nature Materials*. **5**, 204 (2006)
- [7] W. Siemons, G. Koster, H. Yamamoto, W. A. Harrison, G. Lucovsky, T. H. Geballe, D. H. A. Blank, and M. R. Beasley, *Physical Review Letters*. **98**, 196802 (2007)
- [8] A. Kalabukhov, R. Gunnarsson, J. Börjesson, E. Olsson, T. Claeson, and D. Winkler, *Physical Review B*. **75**, 121404 (2007)
- [9] Y. Chen, N. Pryds, J. E. Kleibeuker, G. Koster, J. Sun, E. Stamate, B. Shen, G. Rijnders, and S. Linderöth, *Nano Letter*. **11**, 3774 (2011)
- [10] P. R. Willmott, S. A. Pauli, R. Herger, C. M. Schlepütz, D. Martocchia, B. D. Patterson, B. Delley, R. Clarke, D. Kumah, C. Cionca, and Y. Yacoby, *Physical Review Letters*. **99**, 155502 (2007)
- [11] B. Förg, C. Richter, and J. Mannhart, *Applied Physics Letters*. **100**, 053506 (2012)
- [12] M. Hosoda, Y. Hikita, H. Y. Hwang, and C. Bell, *Applied Physics Letters*. **103**, 103507 (2013)
- [13] D. W. Reagor, and V. Y. Butko, *Nature Materials*. **4**, 593 (2005)
- [14] D. Kan, T. Terashima, R. Kanda, A. Masuno, K. Tanaka, S. Chu, H. Kan, A. Ishizumi, Y. Kanemitsu, Y. Shimakawa, and M. Takano, *Nature Materials*. **4**, 816 (2005)
- [15] H. Gross, N. Bansal, Y. S. Kim, and S. Oh, *Journal of Applied Physics*. **110**, 073704 (2011)
- [16] C. W. Schneider, S. Thiel, G. Hammerl, C. Richter, and J. Mannhart, *Applied Physics Letters*. **89**, 122101 (2006)
- [17] N. Banerjee, M. Huijben, G. Koster, and G. Rijnders, *Applied Physics Letters*. **100**, 041601 (2012)
- [18] C. Cen, S. Thiel, G. Hammerl, C. W. Schneider, K. E. Andersen, C. S. Hellberg, J. Mannhart, and J. Levy, *Nature materials*. **7**, 298 (2008)
- [19] C. Cen, S. Thiel, J. Mannhart, and J. Levy, *Science*. **323**, 1026 (2009)
- [20] P. P. Aurino, A. Kalabukhov, N. Tuzla, E. Olsson, T. Claeson, and D. Winkler, *Applied Physics Letters*. **102**, 201610 (2013)
- [21] M. Kawasaki, K. Takahashi, T. Maeda, R. Tsuchiya, M. Shinohara, O. Ishiyama, T. Yonezawa, M. Yoshimoto, and H. Koinuma, *Science*. **266**, 1540 (1994)
- [22] G. Koster, B. L. Kropman, G. Rijnders, D. H. A. Blank, and H. Rogalla, *Applied Physics Letters*. **73**, 2920 (1998)
- [23] M. Huijben, G. Rijnders, D. H. A. Blank, S. Bals, S. V. Aert, J. Verbeeck, G. V. Tendeloo, A. Brinkman, and H. Hilgenkamp, *Nature Materials*. **5**, 556 (2006)
- [24] G. Rijnders, G. Koster, D. H. A. Blank, and H. Rogalla, *Applied Physics Letters*. **70**, 1888 (1997)